

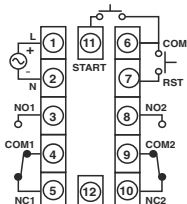


SPECIFICATIONS

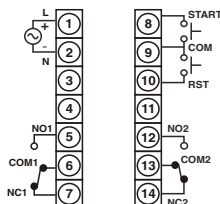
- Display** : Dual, 3 digit seven segment LED display
- Supply** : 85 to 270V AC, 50/60 Hz
24V AC / DC (Optional)
- Operating Modes** : On Delay, Interval, Cyclic On first & Cyclic Off first
- Time Ranges** : 9.99 / 99.9 / 999sec
9.59 min:sec, 99.9 / 999 min,
9.59 hour:min, 99.9 / 999 hour
- Counting Direction** : Down
- Relay Rating** : 5A@250V AC / 28V DC
- Start Input** : Pulse, Gate (Programmable)
- Reset** : On interruption of power, front panel reset & terminal reset
- Outputs** : 2 ; 1 C/O (SPDT)
- Memory Retention** : 10 years
- Accuracy** : **Setting** : $\pm 0.05\%$ of set time or 50 msec (Whichever is greater)
Repeat : $\pm 0.05\%$
- Temperature** : **Operating** : 0 to 50°C
Storage : -20 to 75°C
- Humidity** : 95% RH
- Housing** : PC tinted black
- Weight** : **XT546** : 140 gms
XT246 : 190 gms
XT346 : 240 gms

TERMINAL CONNECTIONS

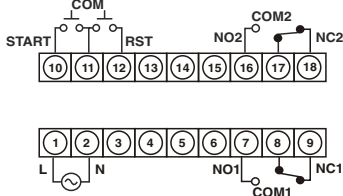
XT546



XT246



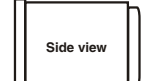
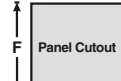
XT346



MECHANICAL INSTALLATION

For installing the Timer

1. Prepare the panel cutout with proper dimensions as shown below :

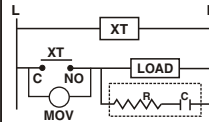
Outline Dimensions (in mm)					Panel cutout Dimensions (in mm)			
 Front bezel		 Side view			 Panel Cutout			
B		C			G			
A		D			F			
E								

MODELS	DIM	A	B	C	D	E	F	G
XT546		48	48	94	45	4	46	46
XT246		72	72	83.7	67	10	69	69
XT346		96	96	73	90.5	10	92	92

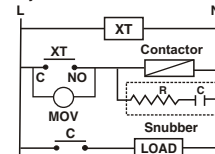
2. Remove the clamp from the controller and push the controller into the panel cutout. Insert the clamp from the rear side until the main is securely fit into the panel.

LOAD CONNECTIONS

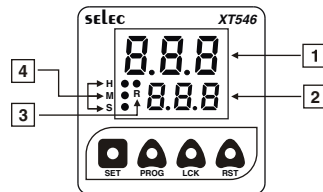
For load current less than 0.5A



For bigger loads, use interposing relay / contactor



FRONT PANEL DESCRIPTION

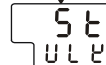


	On line	Config	Lock	For Reset
1	Process Time	Parameter name		
2	Set Time	Parameter setting		
3	O/P Status (Lit when O/P is ON)			
4	Time Range (Blink in online mode)			

PROTECTION LEVEL

NOTE : Press **□+Δ** (LCK) key together continuously for 3sec. to enter into protection level.

Set time Lock



Use **Δ** (any of 3) to select set time LOCK & UNLOCK
Default : UNLOCK

Config. Lock



Use **Δ** (any of 3) to select config. LOCK & UNLOCK
Default : UNLOCK

The unit will auto exit lock mode after 30sec. of key inactivity or by pressing **□+Δ** (LCK) keys continuously for 3sec. to exit the function.

1. Enter configuration by pressing the key + (PROG) key together for 3 sec.
2. Scroll various function ranges by pressing key (any of 3)
3. Scroll various parameter by pressing the key.

LC2
000

Prompt only if configuration Lock enabled in PROTECTION LEVEL
Lock code = 85 [Fixed]

Set key

50 d

50 d

7-5
999

7-5
999

OFF

OFF

5 6 7

5 6 7

FPN

FPN

PO7

PO7

df

df

NOTE : Press **■+▲ (RST)** key together continuously for 5sec. to enter into function.

75t
dne

The unit will auto exit reset mode after 1 sec.

Note : Press key to change the set value. The corresponding digit 9 and then will roll over back to 0.

Set 1st digit

Set 2nd digit

Set 3rd digit

Only if mode selected is cyclic

Set 1st digit

Set 2nd digit

Set 3rd digit

Set 1st digit

Set 2nd digit

Set 3rd digit

NOTE : If the set value is 000 then timer must hold (not work).
All indications will be OFF.

The unit will auto exit set value mode after 30sec. of key inactivity

START : Pulse / Gate

B) Gate : Timing starts at power on. When the **START** and **COMMON** terminal is closed timing freezes and it resumes only when the shorting is opened.

1. On delay. Interval modes :

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Timing diagram for the output of the 74VHC123. The diagram shows the relationship between Supply, Start, Reset, Output ON Delay, and Output Interval. The Set time (t) is indicated for the Start signal. The Output ON Delay is the time from the Start signal to the output going high. The Output Interval is the time from the output going high to the output going low. The diagram shows three cycles of the output signal.

2. Cyclic ON first, Cyclic OFF first modes :

Typical application of Continuous start and reset in On delay mode :

Typical application of Gate start

The diagram shows the timing relationships for a D flip-flop. The signals are Supply, Gate, Reset, and Output. The setup time t_1 is the time before the Gate signal that the Data input must be stable. The hold time t_2 is the time after the Gate signal that the Data input must remain stable. The output delay time t_3 is the time from the rising edge of the Gate signal to the output becoming valid. The total time from the setup of the data to the output becoming valid is $t_1 + t_3$. The time from the hold of the data to the output becoming invalid is t_2 .

(Specifications are subject to change, since development is a continuous process)

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Doc. Name : Operating/1112/XT546/246/346 OP288-V03 (Page 2 of 2)